REMARKS

I. Introduction

Claims 10 to 19 are pending in the present application. In view of the following remarks, it is respectfully submitted that all of the presently pending claims are allowable, and reconsideration is respectfully requested.

II. Rejection of Claim 19 Under 35 U.S.C. §112

Claim 19 was rejected under 35 U.S.C. §112 wherein it is alleged that the feature "depositing on polycrystalline region on the polycrystalline starting layer" does not have proper antecedent basis.

Applicants have amended claim 19 as suggested by the Examiner in the January 10, 2005 Office Action. Applicants respectfully submit that amended claim 19 is in conformance with 35 U.S.C. §112 and respectfully request withdrawal of the rejection.

III. Rejection of Claims 10, 12 to 15, 17 and 18 Under 35 U.S.C. § 102(e) and 35 U.S.C. §103(a)

Claims 10, 12 to 15, 17 and 18 were rejected under 35 U.S.C. § 102(e) as anticipated by, or in the alternative, under 35 U.S.C. §103(a) as obvious over U.S. Patent No. 6,067,858 ("Clark et al."). Applicants respectfully submit that Clark et al. do not anticipate or render obvious claims 10, 12 to 15, 17 and 18 for the following reasons.

Claim 10 relates to a micromechanical component, comprising: a substrate, a micromechanical functional plane provided on the substrate, a covering plane provided on the micromechanical functional plane; and a printed circuit trace plane provided on the covering plane; wherein the covering plane includes a first monocrystalline region epitaxially grown on an underlying second monocrystalline region and a first polycrystalline region epitaxially grown on an underlying first polycrystalline starting layer at the same time.

In contrast to the features provided above, Clark et al. illustrates, in Figure 24, a bottom substrate 600 which is a handle wafer 602 made of a single-crystalline silicon, with an oxide layer 604, and thereon, a polysilicon layer 606, which is patterned, a top substrate (SOI) 610, which is joined to the bottom substrate 600, a top substrate that is thinned back, down to single-crystalline silicon layer 614, an integrated circuitry produced on layer 614; MEMS structures produced in layer 614 by introduced trenches 636, a capping wafer 640 (glass or oxidized silicon) which is bonded to the top substrate 610. Clark et al. does not show or illustrate a covering plain made of mono and polycrystalline silicon, but rather a

capping wafer 640 made of glass or oxidized silicon. Clark et al. does not show a printed circuit trace on capping wafer 640, but integrated circuitry on the micromechanical functional layer 614. Accordingly, in view of this discussion, Clark et al. fails to disclose or suggest the features of claim 10. Applicants respectfully request withdrawal of the rejection to claim 10.

Claims 11 to 18 depend from claim 10 and therefore include all of the features of claim 10. Applicants respectfully submit that claims 11 to 18 are patentable for at least the reasons presented above in relation to claim 10.

III. Rejection of Claims 11 and 19 Under 35 U.S.C. §103(a)

Claims 11 and 19 were rejected under 35 U.S.C. §103(a) as obvious over U.S. Patent No. 6,067.858 ("Clark et al.") in view of Silicon Processing for the VLSI Era Volume 1: Processing Technology, Lattice Press, Sunset Beach, CA, USA, pp. 151-156, 1986 ("Wolf et al."). Applicants respectfully submit that combination of Clark et al. and Wolf et al. does not render obvious claims 11 and 19 for the following reasons.

Claims 11 depends from claim 10 and therefore include all of the features of claim 10.

Claim 19 relates to a method for manufacturing a micromechanical component. Claim 19 describes the steps of providing a substrate, providing a micromechanical functional plane on the substrate, providing a covering plane on the micromechanical functional plane, providing a polysilicon starting layer region-wise on the micromechanical functional plane and leaving open region-wise a first monocrystalline region of the micromechanical functional plane, epitaxially depositing a second monocrystalline region on the first monocrystalline region left open and epitaxially depositing on a polycrystalline starting layer at the same time, and providing a printed circuit trace plane on the covering plane.

The addition of Wolf et al. does not cure the critical defects of Clark et al. Wolf et al. relates to silicon processing of the VLSI era. Title. The Office Action alleges that it would have been obvious to combine the disclosures of Clark et al. and Wolf et al. to one of ordinary skill in the art at the time of the invention because Wolf et al. discloses known epitaxial structures and Clark et al. suggests (at col. 24, lines 1 to 10) using "conventional techniques" (and thus structures) to form the micro-mechanical device.

Applicants respectfully submit that the Office Action citing "conventional techniques" expressly does not refer to the micromechanical structure of the present invention but rather to a standard CMOS process for an integrated circuit. The processing of the

micromechanical component, using bonding, trenching, thinning back, deposition, sacrificial etching of the present invention is not conventional and therefore not obvious. As a result, the combination of references, is not obvious.

Applicants furthermore submit that semiconductor process technology does normally not use bonding processes. It is not obvious to replace an MEMS bonding process with a CMOS epitaxy layer as alleged by the Office Action. Wolf et al. uses silane (SiH4) for simultaneous growth since deposition at 630 degrees C would otherwise run at deposition rates that are too low. The present invention, conversely, uses chlorinated Si-compounds but also introduces a polycrystalline starting layer. The present invention, therefore, is structurally different than those described by the combination of references provided by the Office Action. Applicants furthermore submit that the present invention provides final products which are smaller than those of the cited references. Applicants respectfully request withdrawal of the rejections to claims 11 and 19.

IV. Rejection of Claim 16 Under 35 U.S.C. §103(a)

Claim 16 was rejected under 35 U.S.C. §103(a) as unpatentable over Clark et al. in view of U.S. Patent No. 5,075,253 ("Sliwa et al."). Applicants respectfully submit that combination of Clark et al. and Sliwa et al. does not render obvious claim 16 for the following reasons.

Claim 16 depends from claim 10 and therefore includes all the features of claim 10.

Applicants respectfully submit that the "flip chip" technology is not possible with the Clark et al. capping wafer and therefore a person of ordinary skill in the art would not combine the Clark et al. and Sliwa et al. references. The combination of Sliwa's technique with Clark's sensor is technically impossible (as proposed by the Office Action), since the cap in Figure 25G has no plated through holes. An etched hole 646 is positioned to "permit access to bonding pads 648". Contacting is possible only via wire bonding and not via "solder bumps" for "flip chip". The features of claim 16 allow contacting on the upper planar level, and thus flip-chip techniques which are impossible with the combination of references disclosed. As a result of the combination of Sliwa et al. and Clark et al. failing to

disclose or suggest the features of claim 16 and furthermore due to the inability to technically combine the Sliwa et al. and Clark et al. references to disclose the features of claim 16, applicants respectfully request withdrawal of the rejection to claim 16.

V. Conclusion

In light of the foregoing, it is respectfully submitted that all pending claims are in condition for allowance. Prompt reconsideration and allowance of the present application are therefore earnestly solicited.

Respectfully submitted,

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